In the Claims

1. (original) A method for forming a semiconductor device capacitor, comprising:

providing a base dielectric layer;

etching said base dielectric layer to form an opening therein, said opening defined by first and second cross-sectional dielectric sidewalls;

forming a first conductive cross-sectional spacer on said first dielectric sidewall wherein said first conductive spacer forms a portion of a capacitor top plate;

forming a first capacitor cell dielectric layer on said first conductive spacer;

forming a second conductive cross-sectional spacer on said first capacitor cell dielectric layer;

forming a first conductive layer on said second conductive spacer, wherein said second conductive spacer and said conductive layer each form a portion of a capacitor bottom plate;

forming a second cell dielectric layer on said first conductive layer;

forming a second conductive layer on said second cell dielectric layer, wherein said second conductive layer forms a portion of said capacitor top plate; and

forming a conductive feature which electrically connects said first conductive spacer and said second conductive layer.

2. (original) The method of claim 1, further comprising:

prior to etching said base dielectric layer, forming a third conductive layer over a planarized surface of said base dielectric layer;

during said etching of said base dielectric layer to form said opening, etching said third conductive layer to form an opening in said third conductive layer;

forming said first conductive cross-sectional spacer to contact said third conductive layer;

performing an etch which forms a cross-sectional third sidewall from said second conductive layer, said second cell dielectric layer, and said third conductive layer; and

during said formation of said conductive feature:

forming a conformal fourth conductive layer which contacts said second conductive layer and said third conductive layer;

spacer etching said forth conductive layer which forms a third conductive cross-sectional spacer on said third sidewall and electrically connects said first conductive spacer and said second conductive layer through said third conductive layer.

3. (original) The method of claim 2 further comprising forming fourth and fifth conductive cross-sectional spacers from said fourth conductive layer within said opening in said base dielectric layer during said spacer etch of said fourth conductive layer.

4. (original) The method of claim 2 further comprising removing at least a portion of said third conductive layer using a planarizing process prior to forming said second cell dielectric layer.

5. (original) The method of claim 4 further comprising removing a portion of each of said first conductive cross-sectional spacer, said first capacitor cell dielectric layer, said second conductive cross-sectional spacer, and said first conductive layer during said planarizing process.

6. (original) The method of claim 1 further comprising:

prior to etching said base dielectric layer, forming a third conductive layer over a planarized surface of said base dielectric layer;

during said etching of said base dielectric layer to form said opening, etching said third conductive layer to form an opening in said third conductive layer;

forming said first conductive cross-sectional spacer to contact said third conductive layer;

etching said second conductive layer and said second cell dielectric layer to form an opening therein and to expose said third conductive layer;

forming a conductive plug within said opening in said second conductive layer and said second cell dielectric layer, said plug contacting said second conductive layer and said third conductive layer to electrically connect said first conductive spacer and said second conductive layer through said third conductive layer.

7. (original) The method of claim 6 further comprising removing at least a portion of said third conductive layer by a planarizing process prior to forming said second cell dielectric layer.

8. (original) The method of claim 7 further comprising removing a portion of each of said first conductive cross-sectional spacer, said first capacitor cell dielectric layer, said second conductive cross-sectional spacer, and said first conductive layer during said planarizing process.

9. (original) A method used to form a semiconductor device, comprising:

providing a semiconductor wafer substrate assembly comprising a semiconductor wafer and a conductive contact pad overlying said wafer;

forming an etch stop layer on said contact pad;

forming a blanket planarized base dielectric layer on said etch stop layer;

forming a conformal first conductive layer on said planarized base dielectric layer;

etching said conformal first conductive layer and said planarized base dielectric layer to form first and second cross sectional sidewalls in said base dielectric layer which define a recess in said base dielectric layer, wherein said etch exposes said etch stop layer;

forming a second conductive layer which comprises a first conductive spacer on said first sidewall;

forming a first cell dielectric layer on said first conductive spacer and on said etch stop layer;

forming a third conductive layer on said first cell dielectric layer;

spacer etching said third conductive layer and said first cell dielectric layer to form a second conductive spacer from said third conductive layer, to form a cell dielectric spacer from said first cell dielectric layer, and to expose said etch stop layer;

subsequent to said spacer etching said third conductive layer and said first cell dielectric layer, etching said etch stop layer to expose said contact pad;

forming a fourth conductive layer on said second conductive spacer and on said contact pad;

forming a second cell dielectric layer on said fourth conductive layer;

forming a fifth conductive layer on said second cell dielectric layer; and

electrically connecting said first conductive spacer and said fifth conductive layer, wherein said second and fifth conductive layers form a first capacitor plate, and said third and fourth conductive layers form a second capacitor plate interposed between said first conductive spacer and said fifth conductive layer.

10. (original) The method of claim 9 further comprising:

during said formation of said second conductive layer, forming said spacer to contact said first conductive layer;

etching an opening in said second cell dielectric layer and said fifth conductive layer to expose said first conductive layer;

forming a conductive plug within said opening in said fifth conductive layer and said second cell dielectric layer, said plug contacting said first conductive layer and said fifth conductive layer to electrically connect said first conductive spacer and said fifth conductive layer through said first conductive layer.

11. (original) The method of claim 9 further comprising:

performing an etch which forms a third cross-sectional sidewall from said fifth conductive layer, said second cell dielectric layer, and said first conductive layer;

forming a sixth conductive layer over said fifth conductive layer and on said third cross-sectional sidewall; and

spacer etching said sixth conductive layer to form a conductive spacer on said third cross-sectional sidewall which electrically connects said first conductive spacer and said fifth conductive layer.

12. (original) The method of claim 11 further comprising, during said formation of said sixth conductive layer, forming a portion of said sixth conductive layer within said opening in said base dielectric layer, wherein subsequent to spacer etching said sixth conductive layer, a portion of said sixth conductive layer remains in said opening in said base dielectric layer.

13. - 19. (canceled)

20. (new) A method used to form a semiconductor device, comprising:

forming a semiconductor wafer substrate assembly comprising a base supporting layer having a recess therein;

within the recess in the base supporting layer, forming first and second conductive spacers having a first cell dielectric interposed therebetween which electrically isolates the first and second conductive spacers from each other;

forming a first conductive layer electrically connected to the second conductive spacer within the recess;

forming a blanket second conductive layer over the first conductive layer and electrically separated from the first conductive layer by a second cell dielectric layer; and

electrically connecting the first conductive spacer and the blanket second conductive layer to form a storage capacitor, where the first conductive spacer and blanket second conductive layer form a portion of a capacitor top plate and the second conductive spacer and first conductive layer form a portion of a capacitor bottom plate.

21. (new) The method of claim 20 further comprising etching the blanket second conductive layer prior to electrically connecting the first conductive spacer and the blanket second conductive layer.

22. (new) The method of claim 21 further comprising:

during the formation of the base supporting layer:

forming a base dielectric layer and a base conductive layer over the base dielectric layer;

etching the base conductive layer and the base dielectric layer to form the recess in the base supporting layer; and

subsequent to the etching of the blanket second conductive layer, etching the base conductive layer to form a sidewall defined by the blanket second conductive layer and the base conductive layer.

23. (new) The method of claim 22 further comprising forming a third conductive spacer over the sidewall to electrically connect the blanket second conductive layer and the base conductive layer.

24. (new) The method of claim 22 further comprising:

etching the blanket second conductive layer and the base conductive layer to form an opening therein; and

forming a conductive plug within the opening to electrically connect the blanket second conductive layer and the base conductive layer.

25. (new) A method used to form a semiconductor device comprising a storage capacitor having a top plate and a bottom plate, comprising:

forming a first portion of a capacitor top plate comprising a vertically-oriented conductive spacer;

forming a first cell dielectric layer to contact the first portion of the capacitor top plate;

forming a first portion of a capacitor bottom plate comprising a vertically-oriented conductive spacer to contact the first cell dielectric layer;

forming a second portion of the capacitor bottom plate comprising a vertically-oriented layer to contact the first portion of the capacitor bottom plate;

forming a second cell dielectric layer to contact the second portion of the capacitor bottom plate;

forming a second portion of the capacitor top plate to contact the second cell dielectric layer and which comprises a portion which overlies the first portion of the capacitor top plate, the first and second cell dielectric layers, and the first and second portions of the capacitor bottom plate; and

forming a conductive structure which electrically connects the first and second capacitor top plate portions.

26. (new) The method of claim 25 wherein the formation of the conductive structure which electrically connects the first and second capacitor top plate portions comprises:

etching the first and second capacitor top plate portions to form a sidewall comprising the first and second capacitor top plate portions;

forming a blanket conductive layer on the sidewall;

etching the blanket conductive layer to form a conductive spacer which contacts the sidewall and electrically connects the first and second capacitor top plate portions.

27. (new) The method of claim 25 wherein the formation of the conductive structure which electrically connects the first and second capacitor top plate portions comprises:

etching the first and second capacitor top plate portions to form an opening in the first and second capacitor top plate portions; and

forming a conductive plug within the opening in the first and second capacitor top plate portions.

28. The method of claim 25 further comprising:

providing a semiconductor wafer substrate assembly comprising a semiconductor wafer having a conductively-doped region therein;

forming a conductive pad to contact the conductively-doped region of the semiconductor wafer;

during the formation of the first portion of the capacitor bottom plate:

forming a blanket conductive bottom plate layer; and

spacer etching the blanket conductive bottom plate layer to form the first portion of the capacitor bottom plate having an opening therein whereby the conductive pad is exposed through the opening in a bottom of the bottom plate layer; and

forming the second portion of the capacitor bottom plate to contact the first portion of the capacitor bottom plate layer and the conductive pad through the opening in the first portion of the bottom plate layer.